Stability Analysis and Layout Design of an Internally Stabilized Multi-Finger FET for High-Power Base Station Amplifiers

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Abstract — **A high-power, discrete, and internally-matched FET, such as for use in base station amplifiers, consists of lots of gate fingers to realize a very large periphery. It is well-known that many active devices combined in parallel likely form many closed loops and cause odd mode oscillation. However, stability analysis among FET fingers is usually complex, because of the existence of lots of active nodes. In this paper, novel internally stabilized multi-finger FET layout methodology with a branched gate feed structure is proposed, to stabilize among gate fingers without increasing the occupied layout area of the FET. The feature of this layout is that the branched gate feed structure, which can be fabricated without any extra processing step, functions as a resistor to isolate each FET cell. Stability analysis and layout design were achieved by using the NDF (Normalized Determinant Function) evaluation technique, which can deal with lots of active nodes. In an experiment for a GaAs FET of 134 mm gate width with 168 gate fingers, this stability analysis precisely predicted an oscillation frequency of the FET having multiple closed loops. The new approach presented here on the gate feed structure effectively suppressed odd mode oscillation.**

I. Introduction

High-power, discrete, and internally matched FETs are key devices for such as base stations of 3rd generation cellular phone systems and satellite communication systems. These systems demand not only high-power output, good linearity, and efficiency but also cost effectiveness. To achieve high output power, small size, and low cost in FET chips, an inter-digital finger layout is often used for the FET chips.

The inter-digital finger layout directly combines lots of gate fingers in parallel by the gate feed of the bus line. It is well known that many transistors operating in parallel cause odd mode oscillation [1-6]. In particular, the odd mode oscillation occurs in a large periphery transistor for high-power amplifiers. Stability analysis of a large periphery FET with many active nodes is usually very complex, because many combinations of close loops exist among gate fingers. Platzker et al. [1][2] and Mons [3] proposed effective and rigorous methods using NDF (normalized determinant function) evaluation, which can predict odd mode oscillation. This technique is suitable for stability analysis dealing with lots of active nodes. However, these reports only deal with small circuitry, such as MMIC, and no reports have been published on verification on a very large periphery FET with many active nodes, and the interaction among the FET fingers. Moreover, discrete high-power FETs cannot adopt a complex circuit for stabilization, such as in MMICs, because of restriction on the fabrication process and chip size.

This paper presents a stability analysis and a novel multi-finger FET layout design with a branched gate feed structure to avoid instability. The feature of the proposed structure is that the branched gate feed functions as a resistor to isolate each FET finger. This structure can be achieved without any extra processing step, because the branched feed is formed simultaneously in the gate fabrication process. Moreover, this layout is established without chip size extension. This structure is very effective for stabilization of high-power FETs.

II. Stability Analysis on a Multi-Finger FET

Figure 1 shows the NDF calculation method to determine the stability of an N port network [2]. This N port network includes N parts of FET as active nodes. Dependent sources of the FET model are usually controlled by the internal voltage of the gate capacitance. On the NDF calculation, the external voltage source (V_{ext}) is defined as the control voltage of the dependent source. The Return Ratio (RR) of each dependent source is given by

$$RR_n = \frac{-V_{out}}{V_{ext}}, \qquad (1)$$

where V_{out} is the voltage at the both sides of the gate capacitance. The number "n" is the order of a dependent source. When the RR_n is evaluated, the transconductances of the sources from 1 to n-1 order are set to zero. NDF can be expressed as follows:

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$$NDF_n = RR_n + 1. \quad (2)$$

By the equations (1) and (2), NDFs are calculated on each source. The total NDF of all dependent sources (NDF_a), which can determine the stability of the N port Network, is given by

$$NDF_a = NDF_1 \times NDF_2 \times \cdots\cdots \times NDF_N. \quad (3)$$

When the NDF_a plotted on polar plane encircles the origin and crosses the real axis on the left half plane, the N port network is unstable. The cross point on the negative real axis indicates the oscillation frequency.

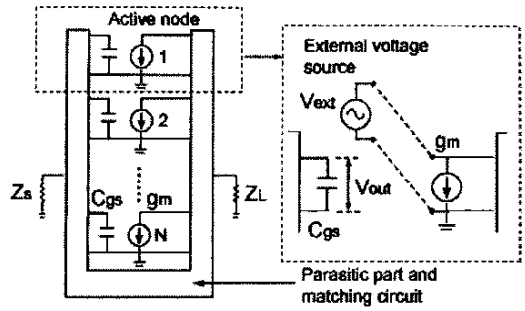


Figure 1. NDF calculation method of multi-port network with N active nodes.

First, the instability of the conventional multi-finger FET was analyzed using the NDF evaluation. Figure 2 shows a large periphery multi-finer FET that adopts the conventional inter-digital FET layout. An AlGaAs/GaAs hetero-structure FET was applied. All gate fingers are directly combined in parallel by the gate feed. The number of gate fingers is 168, and the total gate width is 134 mm. The analysis of odd mode oscillation among FET fingers is very complex, because of including many active nodes.

Figure 3 shows the model for the stability analysis of the multi-finger FET. On the model, the FET is divided into 14 unit cells, and the small signal equivalent parameters of the FET are extracted for a single cell. To evaluate the stability among the paralleled combined fingers, the gate feed is added between neighboring FET cells, where the feed can be modeled as a series-connected resistor and inductor. The input and output matching circuits are microstrip lines formed on the high dielectric substrates. The port of the microstrip matching network connected by wires to the bonding pads of the FET is divided into 14 ports, to analyze the interaction among unit cells. S-parameters of both circuits with the multi-port are calculated using the electromagnetic field simulation. The NDF of the network including the multi-finger FET can be calculated using these models.

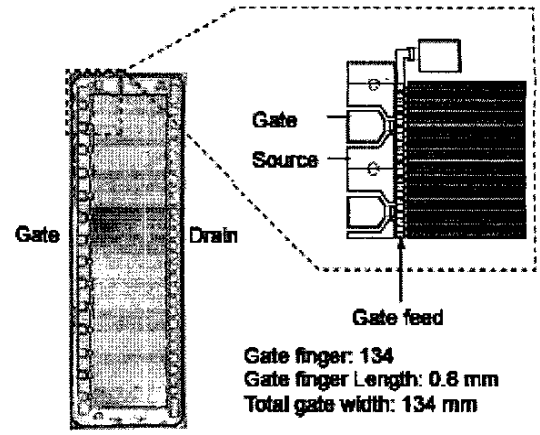
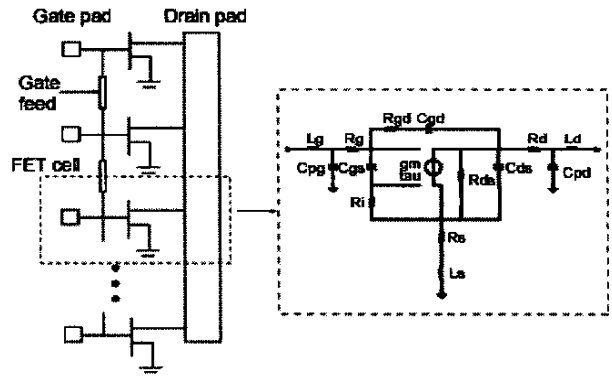


Figure 2. Inter-digital layout of Multi-finger FET.



The NDF of this network, calculated by equation (3), is shown in Figure 4. The current sources in equivalent circuit model of the unit cell FET correspond to the dependent sources shown in Figure 1. The calculation of the NDF was performed upon a commercial CAD tool, Agilent ADS. The frequency of the cross point on the negative real axis is 3.65 GHz. This result indicates instability of 3.65 GHz.

The measured oscillation spectrum is shown in Figure 5. This circuit exhibits a strong oscillation at 3.65 GHz when the DC bias is supplied without the RF input signal. The experimental result is in good agreement with the above-mentioned NDF calculation.

Figure 6 shows the stability factor K and MSG/MAG, calculated on the two port S-parameters of the same circuit. The K factor is over 1, at 3.65 GHz. This result indicates that the K factor does not detect the instability at 3.65 GHz.

This analysis model can predict instability in a multi-finger FET with many active nodes.

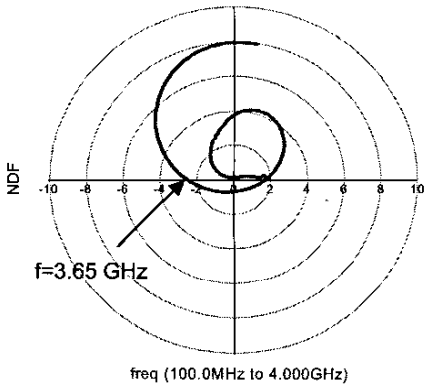


Figure 4. NDF of the network.

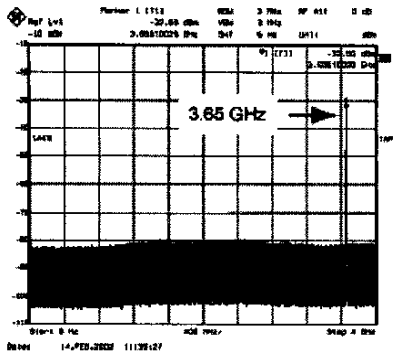


Figure 5. Measured oscillation spectra of the multi-finger FET. (Vd=3V, Id=300mA)

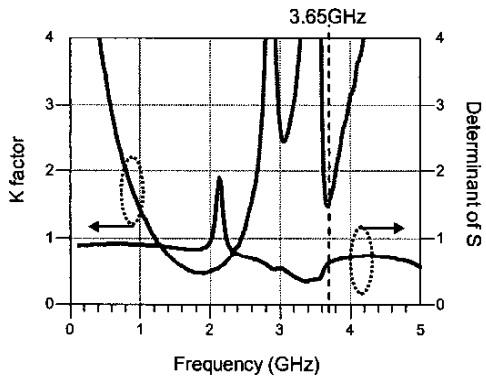


Figure 6. Simulated K factor and Determinant of S. (Vd=3V, Id=300mA)

III. Multi-Finger FET Layout Design To Suppress Instability

The results of stability analysis show that odd mode oscillation occurs among the gate fingers in a multi-finger FET. To suppress the instability, the insertion of isolation resistance among the gate fingers on the chip is most effective in general, but the insertion of an ion implantation resistor or a thin film resistor expands the chip size. To overcome this problem, a new gate feed pattern is proposed in the multi-finger FET.

Figure 7 shows the conventional gate feed layout (a), and the novel gate feed one to avoid instability (b). In the conventional layout, the gate feed directly connects gate fingers, while in the novel layout, the gate feed is partitioned by gaps in the feed, and added branched gate feeds connect the two cells. These branched gate feeds function as isolation resistors. All elements of this feed structure consist of the same Au/WSi metal layer to the gate fingers. The sheet resistance of Au/WSi metal layer is 0.05 Ohms. The width of the gate feed can be controlled precisely in the gate fabrication process. Therefore, the resistance of the branched feed can be controlled by changing its width and length, precisely and easily. Moreover, this branched feed, which can be arranged in the space between RF bonding pads and gate fingers, is very compact and does not involve chip size expansion.

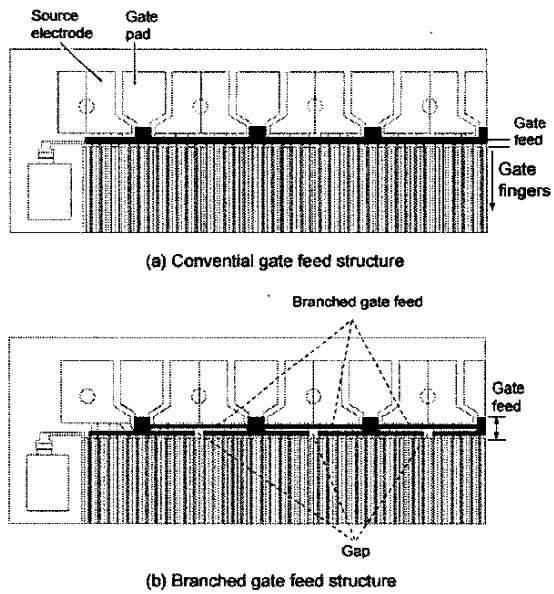


Figure 7. Branched gate feed pattern for suppressing oscillation.

To determine the optimum resistance value of the branched gate feed to avoid oscillation, the NDFs of the multi-finger FET with isolation resistances are calculated. Figure 8 shows the dependence of NDF on the isolation resistance (R_f) of branched gate feeds. An FET model with isolation resistances is used for this calculation. In accordance with the increase of the resistance from 3 to 10 Ohm, the NDF_a plots have no cross point on the negative real axis, which indicates a stable state, but the instability increases at over 100 Ohms resistance reversely. The resistance of the branched gate feed was determined to be 5 Ohms to obtain a simple layout of gate branched feed.

On the experimental result, the oscillation at 3.65 GHz was suppressed in the multi-finger FET that has the new gate feed structure. It is confirmed that the novel gate feed structure is effective to suppress oscillation.

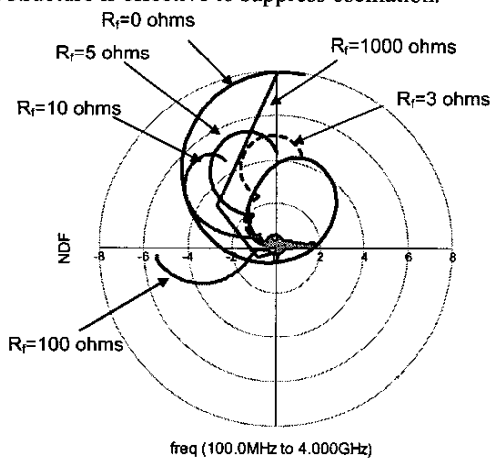


Figure 8. NDF depending on the isolation resistance.

Finally, the effect of the proposed gate feed pattern on the power characteristics was experimentally verified. Figure 9 shows the measured power performance of the 160W FET composed of the internally stabilized FETs for the W-CDMA base station. The drain voltage and the quiescent current was 12 V and 4 A, respectively. The operation frequency was 2.1 GHz. To verify the influence on the RF performance of the new structure, the characteristics of the conventional FET are also shown in the figure. The 4 FET chips are combined in a package with a matching circuit. The output power and gain are not changed by the new gate feed structure. The maximum output power and the linear gain are 52.4 dBm and 12.5 dB, respectively. The influence of the gate feed can be ignored on the RF power performance.

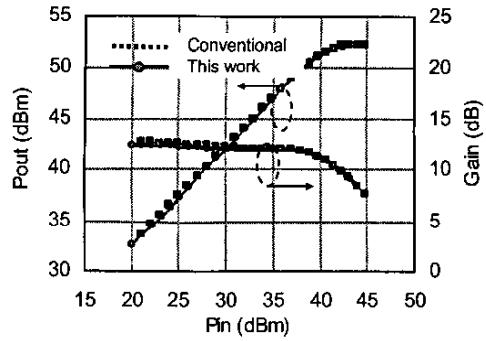


Figure 9. Power performance of 160W internally matched FET for W-CDMA application.

V. Conclusion

A novel and practical internally stabilized multi-finger FET with a branched gate feed structure is proposed here. It successfully achieves suppression of instability and the compact stabilization circuit for high-power amplifiers. Stability analysis of a large periphery multi-finger FET based on NDF evaluation technique can predict the frequency of odd mode oscillation generated among FET fingers. This method was applied to the layout design of the internally stabilized multi-finger FET layout. Moreover, it was verified experimentally that this structure does not have a harmful influence on RF performance. This approach is effective and practical for high-power amplifiers.

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